

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

 Search Results[BROWSE](#)[SEARCH](#)[IEEE Xplore® GUIDE](#)

Results for "(debugging <and>debug registers<and>parallel) <and> (pyr >= 1951 <and> pyr <= 2)"
Your search matched 1 of 1222090 documents.

[e-mail](#)

A maximum of 500 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.

» Search Options[View Session History](#)[Modify Search](#)[New Search](#) [»](#)**» Key****IEEE JNL** IEEE Journal or Magazine**IEE JNL** IEE Journal or Magazine**IEEE CNF** IEEE Conference Proceeding**IEE CNF** IEE Conference Proceeding**IEEE STD** IEEE Standard Check to search only within this results setDisplay Format: **Citation** **Citation & Abstract** **1. Cut-based functional debugging for programmable systems-on-chip**

Kirovski, D.; Potkonjak, M.; Guerra, L.M.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

Volume 8, Issue 1, Feb. 2000 Page(s):40 - 51

Digital Object Identifier 10.1109/92.820760

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(344 KB\)](#) | [IEEE JNL](#)**Indexed by**
[Help](#) [Contact Us](#) [Privacy & :](#)

© Copyright 2005 IEEE -

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

 Search Results[BROWSE](#)[SEARCH](#)[IEEE Xplore GUIDE](#)

Results for "(port<and>debug registers<and>parallel) <and> (pyr >= 1951 <and> pyr <...)"

[e-mail](#)

Your search matched 1 of 1222090 documents.

A maximum of 500 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.» **Search Options**[View Session History](#)**Modify Search**[New Search](#) [»»](#)» **Key****IEEE JNL** IEEE Journal or Magazine**IEE JNL** IEE Journal or Magazine**IEEE CNF** IEEE Conference Proceeding**IEE CNF** IEE Conference Proceeding**IEEE STD** IEEE Standard Check to search only within this results setDisplay Format: **Citation** **Citation & Abstract** **1. Cut-based functional debugging for programmable systems-on-chip**Kirovski, D.; Potkonjak, M.; Guerra, L.M.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 8, Issue 1, Feb. 2000 Page(s):40 - 51
Digital Object Identifier 10.1109/92.820760[AbstractPlus](#) | [References](#) | [Full Text: PDF\(344 KB\)](#) | [IEEE JNL](#)[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -

Indexed by
Inspec



□ Search Results

BROWSE

SEARCH

IEEE Xplore GUIDE

Results for "(debug registers) <and> (pyr >= 1951 <and> pyr <= 2001)"

Your search matched 5 of 1222090 documents.

A maximum of 500 results are displayed, 25 to a page, sorted by Relevance in Descending order.

✉ e-mail

» Search Options

[View Session History](#)

Modify Search

[New Search](#)

(debug registers) <and> (pyr >= 1951 <and> pyr <= 2001)

»

 Check to search only within this results setDisplay Format: Citation Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

Select Article Information

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

- 1. Considerations for implementing IEEE 1149.1 on system-on-a-chip integr

Oakland, S.F.;

Test Conference, 2000. Proceedings. International

3-5 Oct. 2000 Page(s):628 - 637

Digital Object Identifier 10.1109/TEST.2000.894257

[AbstractPlus](#) | [Full Text: PDF\(716 KB\)](#) IEEE CNF

IEEE STD IEEE Standard

- 2. Functional debugging of systems-on-chip

Kirovski, D.; Potkonjak, M.; Guerra, L.M.;

Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IF International Conference on

8-12 Nov 1998 Page(s):525 - 528

[AbstractPlus](#) | [Full Text: PDF\(536 KB\)](#) IEEE CNF

- 3. Constructing high level macrocell models using the Shlaer-Mellor method

Whipp, D.;

Solid-State Circuits Conference, 1997. ESSCIRC '97. Proceedings of the 23rd

16-18 Sept. 1997 Page(s):376 - 379

[AbstractPlus](#) | [Full Text: PDF\(20 KB\)](#) IEEE CNF

- 4. Cut-based functional debugging for programmable systems-on-chip

Kirovski, D.; Potkonjak, M.; Guerra, L.M.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on

Volume 8, Issue 1, Feb. 2000 Page(s):40 - 51

Digital Object Identifier 10.1109/92.820760

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(344 KB\)](#) IEEE JNL

- 5. Framework for testing the fault-tolerance of systems including OS and ne

Buchacker, K.; Sieh, V.;

High Assurance Systems Engineering, 2001. Sixth IEEE International Sympos

22-24 Oct. 2001 Page(s):95 - 105

Digital Object Identifier 10.1109/HASE.2001.966811

[AbstractPlus](#) | [Full Text: PDF\(164 KB\)](#) IEEE CNF

[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) |

Welcome United States Patent and Trademark Office

[□ Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE Xplore GUIDE](#) [e-mail](#)

Results for "(debug control registers) <and> (pyr >= 1951 <and> pyr <= 2001)"

Your search matched 0 documents.

A maximum of 500 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.» [Search Options](#)[View Session History](#)[Modify Search](#)[New Search](#) » [Key](#)

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

 Check to search only within this results setDisplay Format: Citation Citation & Abstract**No results were found.**

Please edit your search criteria and try again. Refer to the Help pages if you need assistance.

[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -

Indexed by
 Inspec